REMARKS

I. Introduction

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

Claims 99-105, 450, 456-466 and 475-507 are now pending in this application. Claims 499-507 have been withdrawn from consideration. Claims 99, 450, 456, 475 and 499 are written in independent form. No claims have been added, canceled or amended.

II. The § 103(a) Rejections Should Be Withdrawn

Claims 99-105, 450, 456-466 and 475-498 have been rejected under § 103(a) as being unpatentable over Watanabe (U.S. Patent No. 5,091,762) in view of Uochi (U.S. Patent No. 6,028,326) together or further in view of other references, as provided in more detail below. This rejection is respectfully traversed because there is no motivation to combine Watanabe and Uochi for the reasons provided in more detail below. Applicants respectfully request a withdrawal of all § 103(a) rejections because the rejections of independent claims 99, 450, 456 and 475 are all based on an improper combination of Watanabe and Uochi.

A. Independent Claims 450 and 456

Claims 450, 456, 489 and 491 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe (U.S. Patent No. 5,091,762) and Uochi (U.S. Patent No. 6,028,326). Claims 457 to 463, 465, 466, 489 to 491 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe and Uochi, as applied to Claim 456 above, and in further view of Zhang (U.S. Patent No. 5,835,396). These rejections are respectfully traversed.

The present Office Action adds a new reference, Uochi, to the §103(a) rejections made in the previous Office Action. Uochi teaches metal catalyst induced crystallization of an amorphous silicon layer on a glass substrate to form a TFT with a polycrystalline silicon

(i.e., polysilicon) active layer. The metal catalyst reduces the crystallization temperature and time to allow polycrystalline active layer TFTs to be formed on a glass substrate at a low temperature in a short amount of time.

In contrast, Watanabe teaches forming epitaxial (i.e., single crystal) silicon active layers over a silicon substrate. Thus, there is no reason to crystallize the active layers of Watanabe because they are already single crystal.

The Office Action asserts that the motivation to combine Uochi with Watanabe is that the metal crystallized polysilicon layer of Uochi has a high mobility and is produced at a low temperature in a shorter time. Applicants respectfully disagree because one of ordinary skill in the art would not be motivated by these three reasons to combine Watanabe and Uochi.

1. The single crystal layers of Watanabe have a higher mobility than the polycrystalline silicon layers of Uochi

The metal catalyst crystallized polysilicon layer of Uochi has a higher mobility than an amorphous silicon layer. However, the metal catalyst crystallized polysilicon layer of Uochi has a LOWER mobility than the single crystal silicon layers of Watanabe. In other words, since single crystal silicon layers have a higher mobility than polysilicon layers, one of ordinary skill in the art would not substitute a single crystal silicon layer of Watanabe with a polysilicon layer of Uochi to achieve a higher mobility. Thus, the "higher mobility" noted in the Office Action as one of the reasons to combine Watanabe and Uochi is not a proper motivation to combine these references.

2. The process of Watanabe is shorter than that of Uochi

The epitaxial silicon layers of Watanabe are single crystal as deposited. Therefore, the single crystal silicon layers of Watanabe are formed in one step. Thus, no crystallization anneal of Uochi is needed to form the layers of Watanabe.

In contrast, the silicon layers of Uochi are amorphous as deposited and require an extra catalyst deposition step and an extra crystallization step to be converted to a polysilicon layer. Therefore, the polysilicon layers of Uochi are formed in three steps. One of ordinary

skill in the art would not be motivated to substitute the as-deposited single crystal layers of Watanabe with the crystallized polysilicon layers of Uochi because the process of Watanabe is shorter in duration than that of Uochi.

Applicants note that Uochi teaches that the catalyst induced thermal crystallization of amorphous silicon is faster than non-catalyst induced laser or thermal crystallization of amorphous silicon (see col. 2, lines 1-45 of Uochi.). However, the three step crystallization process of Uochi is not faster than the one step epitaxial silicon layer deposition of Watanabe. Thus, the "shorter times" noted in the Office Action as another one of the reasons to combine Watanabe and Uochi is not a proper motivation to combine these references.

3. Uochi provides no motivation to lower the temperature of Watanabe

The device of Watanabe is formed over a single crystal silicon substrate (col. 5, line 13) which can withstand high process temperatures. Thus, a low processing temperature associated with silicon layers formed on a glass substrate is not required in the process and device of Watanabe. In contrast, the device of Uochi is formed on an inexpensive glass substrate which cannot withstand temperatures above 600 °C (see col. 2, lines 20-30, col. 3, line 68 and col. 7, lines 1-4 of Uochi).

Thus, there is no reason to use a low temperature crystallization anneal of Uochi in the process of Watanabe because it would unnecessarily complicate the device manufacturing of Watanabe by addition extra catalyst deposition and crystallization steps without improved silicon layer properties. The method of Uochi is designed specifically for low temperature glass substrates and there is no motivation in Uochi to use this method in a device of Watanabe which contains epitaxial silicon active layers over a single crystal silicon substrate.

Furthermore, one of ordinary skill in the art would not be motivated to substitute high quality epitaxial silicon of Watanabe with lower quality polycrystalline silicon that is contaminated with the crystallization catalyst metal of Uochi (see col. 5, lines 22-26 of Uochi which describes the catalyst contamination of the channel, source and drain regions). Thus, the "low temperature" noted in the Office Action as the third reason to combine Watanabe and Uochi is not a proper motivation to combine these references.

4. No motivation to combine Watanabe and Uochi

Applicants respectfully request a withdrawal of the § 103(a) rejection of claims 450 and 456 and claims dependent therefrom over Watanabe and Uochi because there is no motivation to substitute the high mobility epitaxial silicon layer of Watanabe that is formed in a single deposition step with a lower mobility polycrystalline silicon layer of Uochi that is formed in three steps and which is contaminated with crystallization catalyst impurities.

B. Independent Claim 475

Claims 464, 475 to 482 and 492 to 498 are rejected to under 35 U.S.C. § 103(a) as obvious over Watanabe, Uochi and Zhang, as applied to Claim 456 above, and in further view of Kub (U.S. Patent No. 6,153,495). This rejection is respectfully traversed.

1. No motivation to combine Watanabe and Uochi

As discussed with respect to claims 450 and 456, there is no motivation to combine Watanabe and Uochi. The secondary references relied upon in the rejection of claim 475, Zhang and Kub, also do not provide any motivation to combine Watanabe and Uochi.

Furthermore, the four reference rejection of claim 475 is based on improper hindsight reconstruction because the Office Action impermissible picks and chooses elements from the prior art references using only the present specification as a template. There is no motivation in the four applied references to pick an choose the discrete elements noted in the Office Action to arrive at the claimed device. Thus, the rejection should be withdrawn at least for these reasons.

2. No motivation to combine Kub with Watanabe/Uochi

In a response filed 7/15/03 to the prior Office Action, Applicants pointed out that Kub teaches that when two wafers are bonded together, the wafer surfaces being bonded should be polished by CMP to improve wafer bonding. In contrast, claim 475 recites a monolithic 3D array. A monolithic 3D array does not use wafer bonding to bond separately formed device levels together, as defined on page 19, lines 10-14 of the present specification:

> The term "monolithic" means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

In other words, Kub teaches a non-monolithic 3D array because Kub teaches to separately form two dimensional arrays and then to bond or package these arrays together to form a non-monolithic 3D array. In contrast, claim 475 recites a monolithic 3D array where the layers of the array are deposited on top of each other rather than formed separately and then bonded together.

There is no motivation to import the CMP method / surfaces of Kub into a monolithic 3D array, because Kub teaches that CMP improves wafer bonding, while a monolithic 3D array excludes bonded wafers.

3. The structure of claim 475 differs from that of Kub

Applicants submit that the monolithic structure of the device of claim 475 is different from that of Kub and that claim 475 is patentable for this additional reason.

The Office Action dated 10/14/03 notes that "monolithic" is a process limitation and that a monolithic 3D array product is indistinguishable from a wafer bonded or packaged 3D array product. Applicants respectfully disagree.

The claimed monolithic 3D array product has a different structure from a wafer bonded or packaged 3D array product, in addition to being made by a different process. In a monolithic 3D array, the layers are deposited upon one another, which results in a high quality interface, such as where most of the atoms align continuously across the boundary or interface between the layers.

In contrast, a wafer bonded 3D array will either include a bonding or glue layer between bonded wafers, or for directly (i.e., electrostatically, thermally or frictionally) bonded wafers, the interface between the bonded wafers would be of poorer quality than an interface

between layers of a monolithic 3D array where the layers are deposited on the underlying layers.

For example, Figure 6 of Kub illustrates directly bonded wafers 80, 95 with a boundary or interface 103 between them. Atoms would not align continuously across the boundary 103 between the adjacent single crystal silicon regions 82 and 96 of respective bonded wafers 80 and 95, since Kub does not disclose good atomic alignment across the boundary or interface 103. In contrast, a high quality atomic interface with epitaxial atomic alignment is observed when one single crystal silicon layer is epitaxially grown on an underlying single crystal silicon layer.

Thus, one of ordinary skill in the art would be able to distinguish a monolithic 3D array from a wafer bonded 3D array based on the quality of the interface between layers and/or based on the presence of a glue or bonding layer. Therefore, the term "monolithic" is not just a process limitation but a structural limitation which distinguishes wafer bonded 3D array products from the claimed monolithic 3D array products.

C. Independent Claim 99

Claims 99 to 101 and 483 to 488 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe and Uochi, as applied to Claim 456 above, and in further view of Matsushita (U.S. Patent No. 5,998,808). Claims 102 to 105 are rejected under 35 U.S.C. § 103(a) as obvious over Watanabe, Uochi and Matsushita, as applied to Claim 99 above, and in further view of Zhang.

As discussed with respect to claims 450 and 456, there is no motivation to combine Watanabe and Uochi. The secondary reference relied upon in the rejection of claim 99, Matsushita, also does not provide any motivation to combine Watanabe and Kub.

The Office Action relies on Matsushita for the teaching of a single crystal silicon substrate. However, it appears that Watanabe already teaches a single crystal silicon substrate (Col. 5, line 13). Thus, Matsushita does not provide motivation to combine Watanabe and Uochi. In contrast, Matsushita teaches away from combining Watanabe and Uochi because

Matsushita teaches forming a three dimensional array of devices, where the device layers are single crystal silicon layers over a single crystal silicon substrate (see abstract of Matsushita). Thus, one of ordinary skill in the art would form device layers in single crystal silicon from the teaching of Matsushita and Watanabe rather than in lower mobility, catalyst contaminated polycrystalline silicon of Uochi.

D. Dependent Claims

Dependent claims 101, 479 and 491 recite a CMP planarized surface. A substantially planar, CMP planarized surface, such as that of claim 491, has a higher degree of planarity than the planarity of the surfaces of as-deposited and unplanarized layers of Watanabe.

Applicants respectfully disagree with the statement on page 4 of the Office Action that CMP is a process rather than a structural limitation. A CMP surface is structurally different in terms of its planarity from the surfaces of the as-deposited and unplanarized layers of Watanabe. Thus, CMP planarization is a structural limitation which further distinguishes claims 101, 479 and 491 from Watanabe.

E. Rejoinder

Applicants respectfully request rejoinder of method claims 499-507 upon allowance of claim 475, as provided in MPEP § 821.04.

III. Conclusion

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested. The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date 1/8/04 By _____

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The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.